David Mallasén Quintana

PhD Student · Computer Engineering

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Education

PhD in Computer Engineering *Madrid*
Complutense University of Madrid *In progress*
- Title: Hardware Platform for the Study of Posit Arithmetic in Scientific and Technical Applications.
- Advisors: Manuel Prieto-Matias and Alberto A. Del Barrio.

MSc in Embedded Systems *Stockholm*
KTH Royal Institute of Technology *November 2022*
- Embedded Platforms track. Average grade of 9.32/10 over 120 ECTS (2 years).
- MSc Thesis: Leveraging Posits for the Conjugate Gradient Linear Solver on an Application-Level RISC-V Core.

BSc in Computer Science and Engineering *Madrid*
Complutense University of Madrid *July 2020*
- Itinerary in Computing. Average grade of 8.71/10 over 240 ECTS (4 years).
- Admission grade of 13.45/14. Awarded 7 distinctions (High Honors, *matrícula de honor*) adding up 66 ECTS credits.
- BSc Thesis: Acceleration Techniques for Chess Piece Recognition.

BSc in Mathematics *Madrid*
Complutense University of Madrid *July 2020*
- Itinerary in Computer Science. Average grade of 7.26/10 over 240 ECTS (4 years).
- Admission grade of 13.45/14. Awarded 2 distinctions (High Honors, *matrícula de honor*) adding up 13.5 ECTS credits.
- BSc Thesis: The k-Additive Core as a Graph Problem.

Professional Experience

Teaching and Research Assistant (*Ayudante*) *Madrid*
Complutense University of Madrid *June 2022 - Now*
Full-time. ArTeCS group in the Department of Computer Architecture and Automation.

Guest PhD Student *Lausanne*
EPFL *February 2023 - July 2023*
Full-time. Embedded Systems Laboratory (ESL).

Research Assistant *Madrid*
Complutense University of Madrid *February 2021 - May 2022*
Full-time. PARNASO project in the ArTeCS group in the Department of Computer Architecture and Automation.
Developing a hardware accelerator based on a RISC-V core in SystemVerilog and its corresponding compiler on LLVM. Integrating native support for the posit number format to efficiently target domain-specific applications.

Intern *Madrid*
Indra *February 2019 - August 2019*
Part-time. Robotic Process Automation (RPA) area of the Advanced Technologies Department at Minsait.

Publications

Peer-Reviewed Journal Publications

D. Mallasén, R. Murillo, A. A. D. Barrio, G. Botella, L. Piñuel, and M. Prieto-Matias, "PERCIVAL: Open-Source Posit RISC-V Core With Quire Capability," *IEEE Transactions on Emerging Topics in Computing*, vol. 10, no. 3, pp. 1241–1252, 2022. **JCR Q1**

Peer-Reviewed Conference Proceedings

D. Mallasén, R. Murillo, A. A. Del Barrio, G. Botella, L. Piñuel, and M. Prieto–Matias, "Customizing the CVA6 RISC-V Core to Integrate Posit and Quire Instructions," in *2022 37th Conference on Design of Circuits and Integrated Circuits (DCIS)*, pp. 01–06, Nov. 2022

R. Murillo, **D. Mallasén**, A. A. Del Barrio, and G. Botella, "Comparing Different Decodings for Posit Arithmetic," in *Next Generation Arithmetic* (J. Gustafson and V. Dimitrov, eds.), vol. 13253, pp. 84–99, Cham: Springer International Publishing, 2022

R. Murillo, **D. Mallasén**, A. A. Del Barrio, and G. Botella, "Energy-Efficient MAC Units for Fused Posit Arithmetic," in *2021 IEEE 39th International Conference on Computer Design (ICCD)*, pp. 138–145, Oct. 2021. **GGS Class 2**

Reports and Preprints (non-peer reviewed)

D. Mallasén Quintana, "Leveraging Posits for the Conjugate Gradient Linear Solver on an Application-Level RISC-V Core," tech. rep., KTH Royal Institute of Technology, 2022

D. Mallasén Quintana, A. A. Del Barrio García, and M. Prieto Matías, "LiveChess2FEN: A Framework for Classifying Chess Pieces based on CNNs," *arXiv:2012.06858 [cs]*, Dec. 2020

D. Mallasén Quintana, "Tecnicas de aceleración para el reconocimiento de piezas de ajedrez," tech. rep., Universidad Complutense de Madrid, June 2020

Awards, Fellowships, & Grants

2021 **Jetson Project of the Month Winner - LiveChess2FEN**, NVIDIA

2020 **Best Computer Science BSc Thesis**, UCM

2019-2020 **Collaboration fellowship to research for 8 months in the ArTeCS group**, Spanish Ministry of Education

2016 **First prize, second year category at the II Programming Contest Ada Byron**, Community of Madrid

Talks and Presentations

Conference Presentations

D. Mallasén, R. Murillo, A. A. Del Barrio, G. Botella, L. Piñuel and M. Prieto-Matias. 2022. "Customizing the CVA6 RISC-V Core to Integrate Posit and Quire Instructions". Presented at the XXXVII Conference on Design of Circuits and Integrated Systems, Pamplona, Spain.

D. Mallasén, R. Murillo, A. A. Del Barrio, G. Botella, L. Piñuel and M. Prieto-Matias. 2022. "PERCIVAL: Open-Source Posit RISC-V Core with Quire Capability". Presented at the 29th IEEE Symposium on Computer Arithmetic, Virtual conference.

Poster Presentations

D. Mallasén. 2022. "Hardware Platform for the Study of Posit Arithmetic". PhD Poster Competition at the XXXVII Conference on Design of Circuits and Integrated Systems, Pamplona, Spain.

D. Mallasén, R. Murillo, A. A. Del Barrio, G. Botella, L. Piñuel and M. Prieto-Matias. 2022. "PERCIVAL: Deploying posits and quire into an application-level RISC-V core". Poster session at the 18th ACACES Summer School, Fiuggi, Italy.

Teaching Experience

Fall 2022 — *UCM*

Operating Systems, Teaching Assistant, BSc Computer Science and Eng. (Y3)
Operating Systems, Teaching Assistant, BSc Video Game Development (Y3)
Technology and Organization of Computer Systems, Teaching Assistant, Computer Science and Eng. (Y2)
Computer Organization, Teaching Assistant, BSc Electronic Communications Eng. (Y2)
Introduction to Computers I, Teaching Assistant, BSc Computer Science and Eng. (Y1)

Service & Professional Development

Development

2022	**Seasonal School on Efficient Circuits and Systems for Brain-Inspired Computing**, IEEE CASS Spain	*Madrid, Spain*
2022	**ACM Europe Summer School on HPC Computer Architectures of AI and Dedicated Applications**, Certificate of Honor for Outstanding Performance, ACM	*Barcelona, Spain*
2022	**18th ACACES Summer School**, HiPEAC	*Fiuggi, Italy*
2021	**XACC PhD School**, Xilinx	*Virtual*
2020	**RISC-V 28nm ASIC Implementation Course**, Universidad Complutense de Madrid	*Madrid, Spain*

Peer Review

Journal of Computational Science, Journal of Systems Architecture

Languages

Spanish: Native speaker.

English: CEFR Level C2. IELTS Academic 8.5 / 9 Overall Band Score taken Dec. 2019.

French: CEFR Level B1.